F.Y.BSc.IT-Sem I- A.T.K.T. Exam-Mar'2023

Dt:- 18/3/23

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FYBSc IT / Sem I / Digital Logic and Applications

Time: 2½ Hours **Marks: 75**

Instructions: (a) All questions are compulsory.
(b) Figure to the right indicate marks
(c) Support answers with diagrams & examples wherever necessary

Q.1 Attempt any 3 of the following: **[15M]**

1. Write short note on input bubbled AND gate and input bubbled OR gate.
2. Convert the following numbers
   $(17E.F6)_{16} = (?)_2$
   $(1100101000011.10100101)_2 = (?)_H$
3. Perform the addition of following binary number (1100010+1010001)
4. Write a short note on error correction and detection code.
5. Convert:
   a. $(62)_{10} = (?)_{excess-3}$
   b. $(577)_{10} = (?)_{BCD}$
   c. $(100110000111)_{BCD} = (?)_{10}$
6. Represent the following binary number using a single precision floating point format.
   $N = (1001010011101)_2$

Q.2 Attempt any 3 of the following: **[15M]**

1. State and prove De Morgan's theorem. Realize it using basic gates.
2. Prove the given Boolean expression using Boolean laws and draw the circuit for it using NAND gates only
   A.B + A'B +A'B' = A' + B
3. Using don't care condition find reduced SOP equation and draw the circuit diagram using basic gates. $F(P,Q,R,S) = \sum m(1,2,3,6,12,14) + d(0,11,13)$
4. Describe how NAND gate is used to build NOT, OR, and AND gates.
5. For the logic expression Y = AB + A'B', obtain the truth table, name the operation performed, realize the operation using AND, OR, NOT gate. Also realize it using NAND gates only.
6. Prove the following
   a. A'BC + AB'C + ABC' + ABC = AB + AC + BC
   b. ((A + A'B) (C + D'))' = A'B' + C'D

Q.3 Attempt any 3 of the following: **[15M]**

1. Design Gray to BCD code converter.
2. Explain full adder in detail.
3. Describe the working of 2 bit half subtractor.
4. Describe the working of a binary multiplier.
5. Define cascading. Design 8:1 multiplexer using two 4:1 multiplexers.
6. Write a short note on priority encoder

Q.4 Attempt any 3 of the following: **[15M]**

1. Draw logic circuit diagram of D flip flop (level triggered) and explain it's working.
2. Briefly describe the architecture of SISO shift register.
3. Write a short note on synchronized counters.
4. How flip flop is used in eliminating keyboard debouncing ? Explain.
5. Explain clocked SR flip flop using four NAND gates.
6. Compare Combinational logic circuits and Sequential logic circuits.

Q.5 Attempt any 3 of the following: **[15M]**

1. With the help of a flow chart explain binary multiplication algorithm.
2. Show the multiplication process using Booth's algorithm when the following binary numbers are multiplied $(-12) \times (-18)$
3. Explain how to divide 13 by 3 in the registers and showing how the quotient and remainder are placed after the division (all are 5 bit registers)
4. Explain the role of ALU as a part of computer system
5. Write a note on Carry Look Ahead Generator
6. Multiply 13×11 using the shift and add method and give the values of all the registers after each step.